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CONFIRMATION NO. 3384

SERIAL NUMBER 10/757,415	FILING OR 371(c) DATE 01/15/2004 RULE	CLASS 703	GROUP ART UNIT 2123	ATTORNEY DOCKET NO. 04173.0441	
APPLICANTS Hisashi Kaneko, Fujisawa-shi, JAPAN; Motoya Okazaki, Tokyo, JAPAN; Hiroyuki Toshima, Saitama-shi, JAPAN;					
** CONTINUING DATA ***** <i>None aye 7/27/07</i>					
** FOREIGN APPLICATIONS ***** JAPAN P2003-344526 10/02/2003 <i>aye 7/27/07</i>					
IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 04/19/2004					
Foreign Priority claimed <input checked="" type="checkbox"/> yes <input type="checkbox"/> no 35 USC 119 (a-d) conditions met <input checked="" type="checkbox"/> yes <input type="checkbox"/> no <input type="checkbox"/> Met after Allowance Verified and Acknowledged <i>aye 7/27/07</i> Examiner's Signature Initials		STATE OR COUNTRY JAPAN	SHEETS DRAWING 10	TOTAL CLAIMS 22/12	INDEPENDENT CLAIMS 4
ADDRESS 22852					
TITLE Simulation circuit pattern evaluation method, manufacturing method of semiconductor integrated circuit, test substrate, and test substrate group					
FILING FEE RECEIVED 1022	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		<input type="checkbox"/> All Fees <input type="checkbox"/> 1.16 Fees (Filing) <input type="checkbox"/> 1.17 Fees (Processing Ext. of time) <input type="checkbox"/> 1.18 Fees (Issue) <input type="checkbox"/> Other _____ <input type="checkbox"/> Credit		